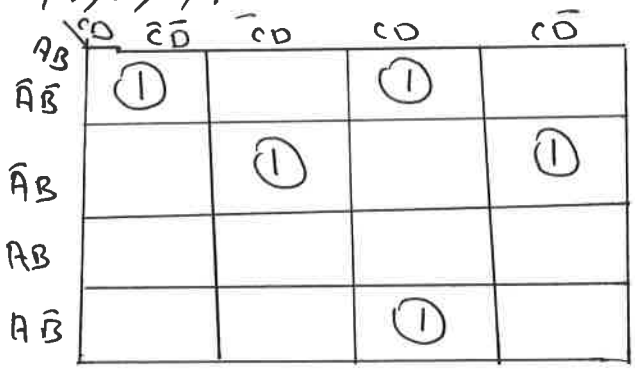
Ex) Design a Logic cct to proved the odd parity bit for BCD (8421) code using NAND gate only?

Sol^ :-

BCD A	B	C	D	P (odd)
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1

$P(odd) = \Sigma\ 0, 3, 5, 6, 9$



$P(odd) = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}B\bar{C}D + \bar{A}BC\bar{D} + A\bar{B}\bar{C}D$

↓

H.W

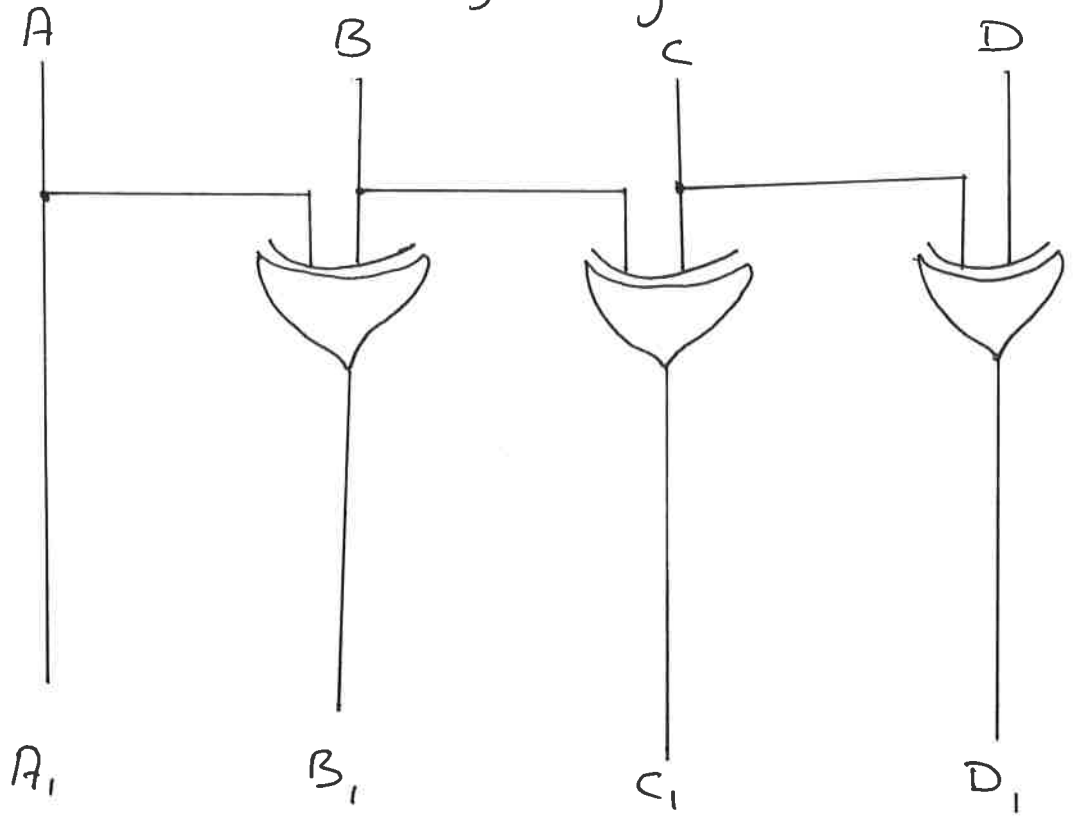
Ex) Design a Logic cct that accepts a 2-bit number and generate o/p binary number equal to the cubic of the i/p ? H.W

Gray Code Convertion :-

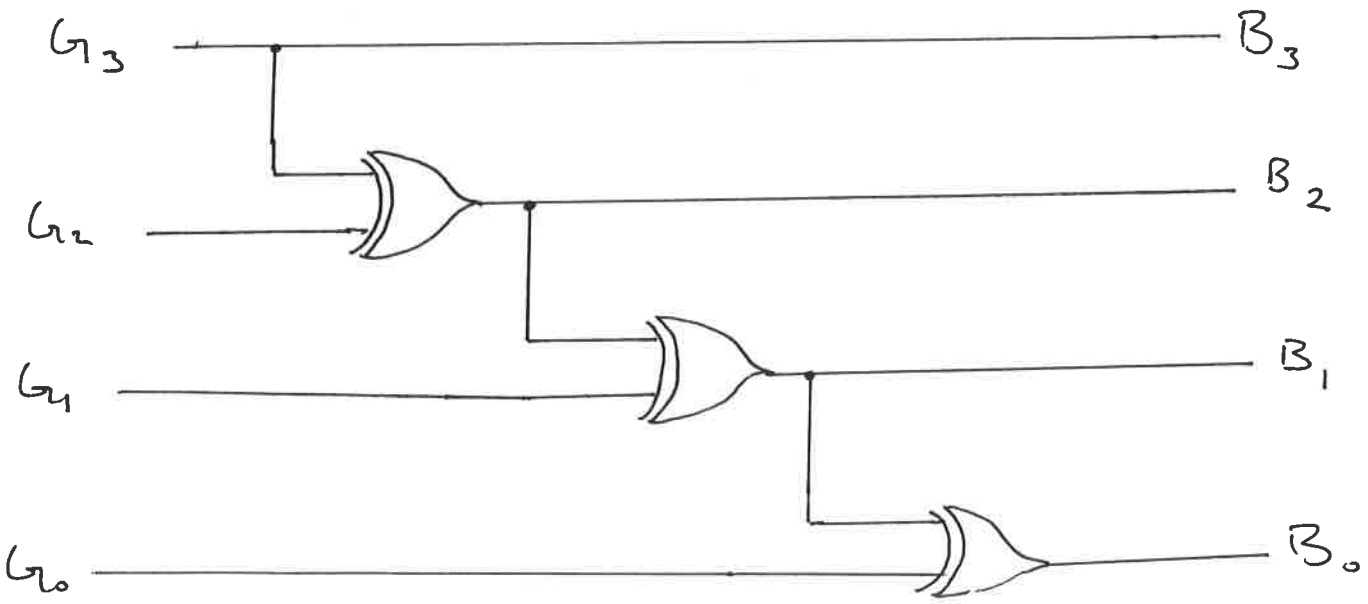
By representing the 10 Decimal digits having 4 bit, we can obtained it's Gray Code.

Decimal Digit	Binary				Gray code			
	A	B	C	D	A_1	B_1	C_1	D_1
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	1	0
5	0	1	0	1	0	1	1	1
6	0	1	1	0	0	1	0	1
7	0	1	1	1	0	1	0	0
8	1	0	0	0	1	1	0	0
9	1	0	0	1	1	1	0	1

This Can be achived by using Ex-OR Gates only.



Gray to Binary Convertion :-



BCD to Binary Conversion :-

One method of BCD to Binary Code conversion involves the use of adder cct.

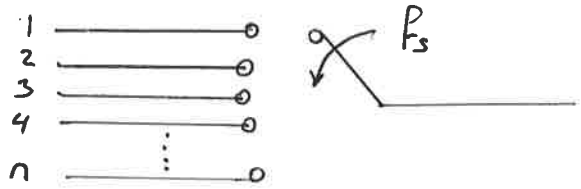
The basic Conversion process is as Follows :-

1- The value of the bit in the BCD number is represented by binary number.

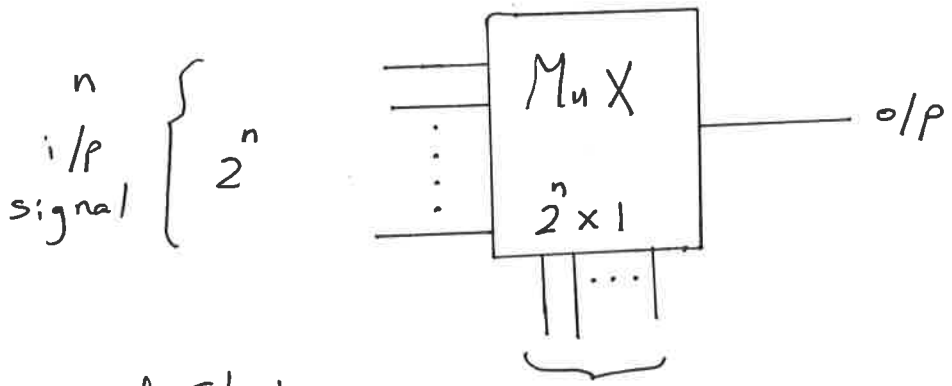
2- All of the binary representations of all bits that are (1's) in the BCD number are added.

3- The result of this addition is the binary equivant of BCD number.

Multiplexer :-



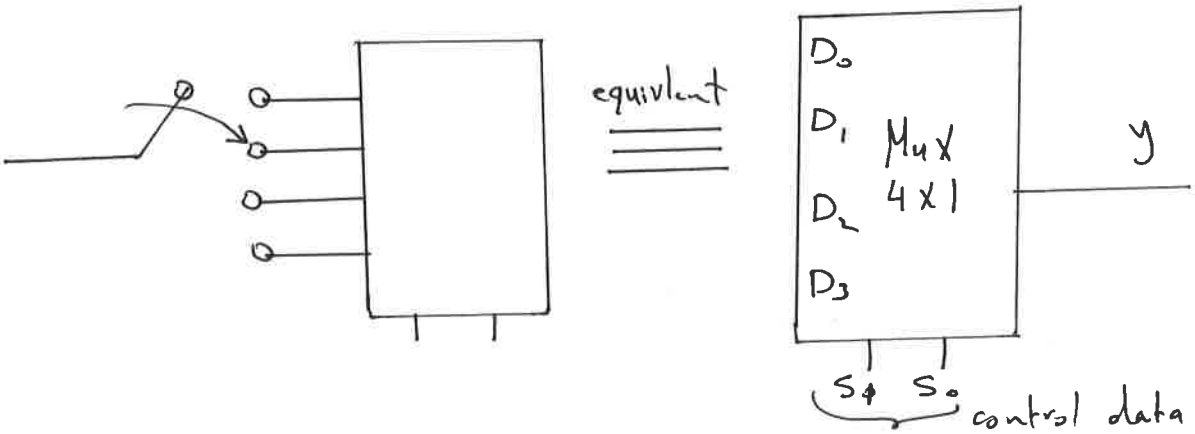
Multiplexer means transmiting along number of channal units over a small number of channel of Lines, the Basic multiplexer has many I/P Lines and Single o/p Line. Normally have 2^n I/P's and n control lines whose bit combination determine which I/P is selected the circuit shown below has (n) and (m) control.



The No. of I/p Line $= 2^n$

No. of control Signal Line = n

The multiplexer may be consider as multi way switch as shown below.



The truth table :-

S_1	S_0	y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

To find the (y) value, it is depent on the (selector), .

When :- 1- IF ($\frac{S_1}{0}$ $\frac{S_0}{0}$), i.e ($y = D_0 \bar{S}_1 \bar{S}_0$), the o/p is ($D_0$).

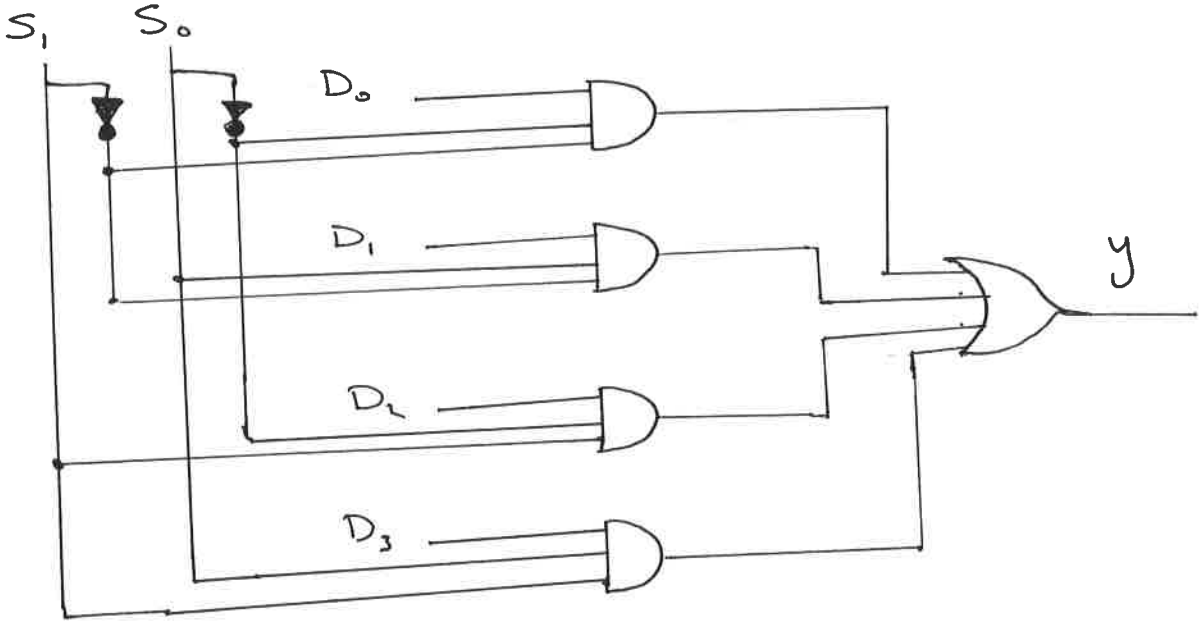
2- IF ($\frac{S_1}{0}$ $\frac{S_0}{1}$), i.e ($y = D_1 \bar{S}_1 S_0$), the o/p is (D_1).

3- IF ($\frac{S_1}{1}$ $\frac{S_0}{0}$), i.e ($y = D_2 S_1 \bar{S}_0$), the o/p is (D_2).

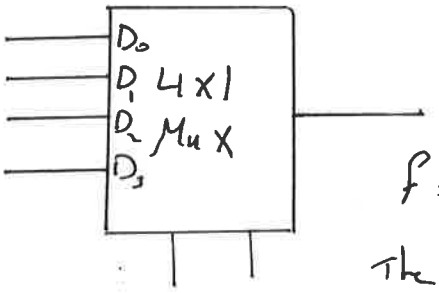
4- IF ($\frac{S_1}{1}$ $\frac{S_0}{1}$), i.e ($y = D_3 S_1 S_0$), the o/p is (D_3).

The Logic cct for

$$y = D_0 \bar{S}_1 \bar{S}_0 + D_1 \bar{S}_1 S_0 + D_2 S_1 \bar{S}_0 + D_3 S_1 S_0$$



Ex) Find the o/p stats for the Mux shown below :-



$f = D_2$

The $S_1 S_0$ is 10

$= D_2 S_1 \bar{S_0}$

The o/p is D_2

Ex) Implement the following Function by means of using 4x1 MuX if $f = \Sigma\, 0, 1, 3, 5, 7$

SoL^:-)

$D_0 \longrightarrow D_7$

$2^n = 8 \Rightarrow n = 3$

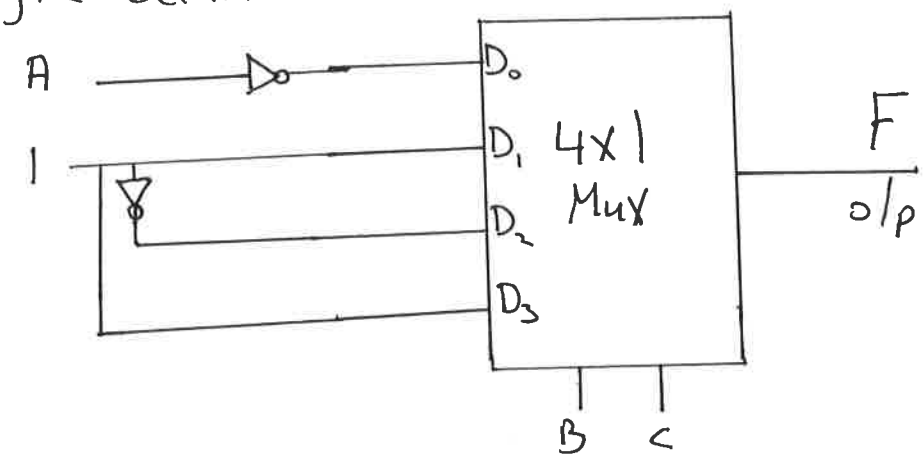
$\therefore D = 8 \quad (A, B, C)$

We choose the A as data i/p & B, C as data Select

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

		D_0	D_1	D_2	D_3
data i/p	$\bar{A}$	(0)	(1)	2	(3)
	A	4	(5)	6	(7)
The result		$\bar{A}$	1	0	1

The Logic cct:-

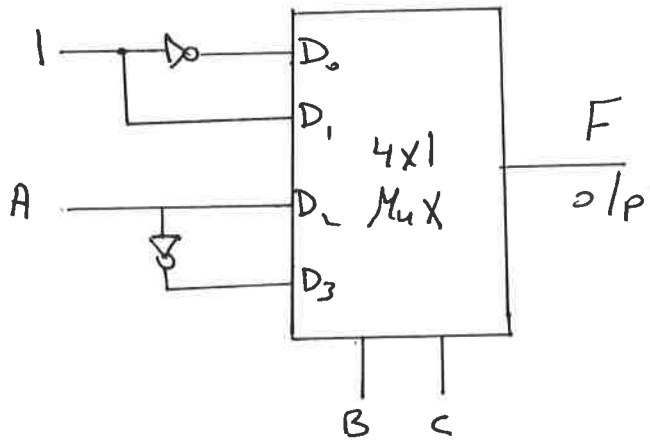


Ex) Implement the following function by means of using 4x1 MuX if $f_s \Sigma$ 1, 3, 5, 6

Sol^)
B, C = Selector
A = Data I/p
MuX = 4x1

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

	D_0	D_1	D_2	D_3
A^-	0	(1)	2	(3)
A	4	(5)	(6)	7
Result	0	1	A	A^-



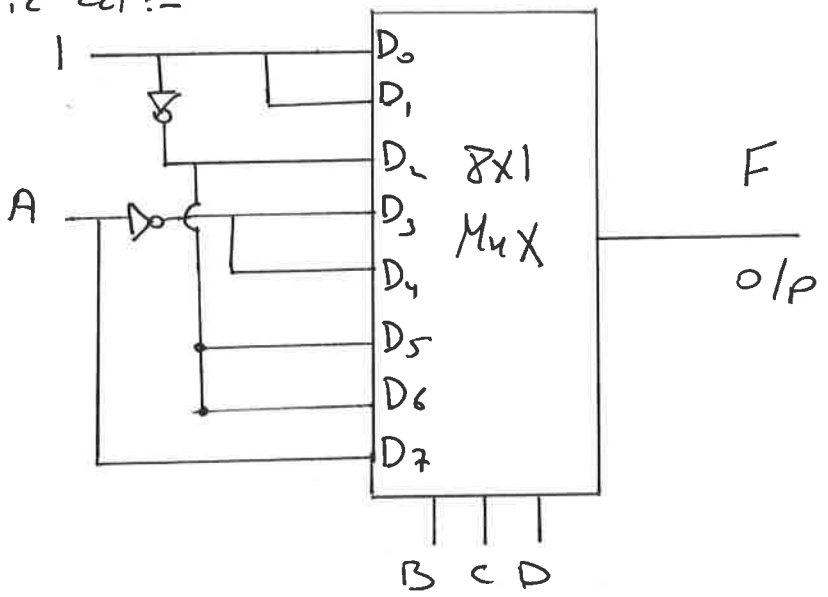
Ex) Implement the following function means of using 8x1 MuX if $f_s \Sigma$ 0, 1, 3, 4, 8, 9, 15

Sol^)

A	B	C	D	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
⋮	⋮	⋮	⋮	⋮

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
A^-	(0)	(1)	2	(3)	(4)	5	6	7
A	(8)	(9)	10	11	12	13	14	(15)
	1	1	0	A^-	$\hat{A}$	0	0	A

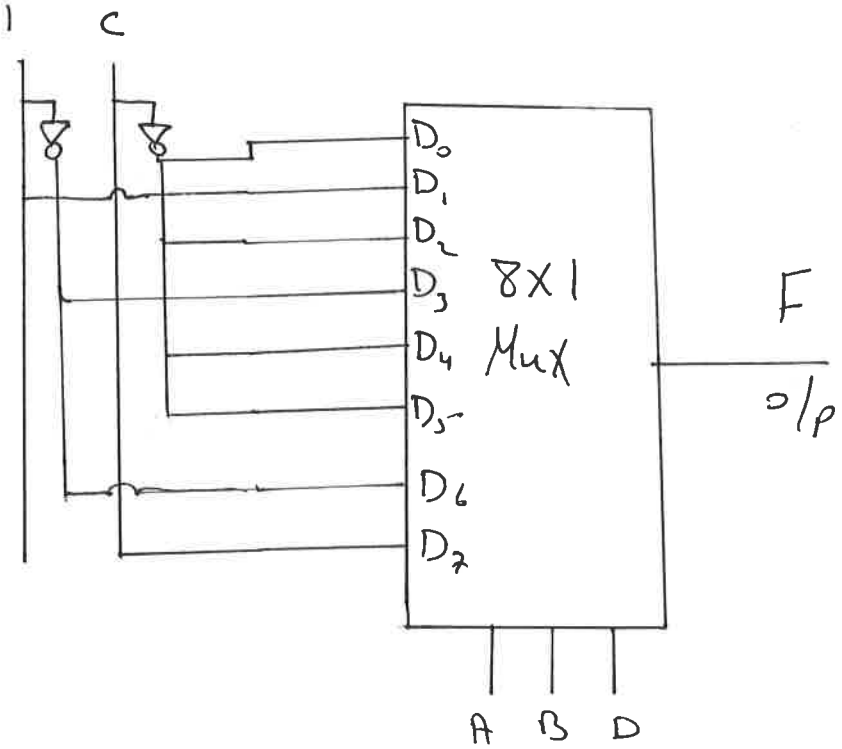
The Logic cct :-



Ex) Repeat the last example and using ABD as Selector with 8x1 MuX.

Sol)

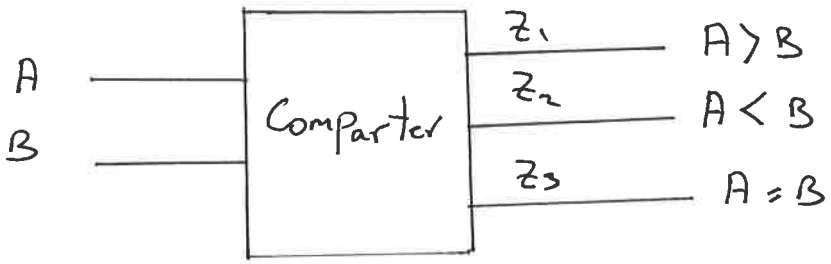
	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$\bar{C}$	(0)	(1)	(4)	5	(8)	(9)	12	13
C	2	(3)	6	4	10	11	14	(15)
	$\bar{C}$	1	$\bar{C}$	0	$\bar{C}$	$\bar{C}$	0	C



Comparater :-

Its a combintional Logic cct having 2 inputs (any two No's) inorder to find there relative magnitude. The outcome of the Comprater is specified by there binary variables which indicate the (A>B), (A<), and (A=B).

The blocks diagram of the Comparator is shown below:-



The comparater is used in digital computers to compare between two numbers, (A,B).

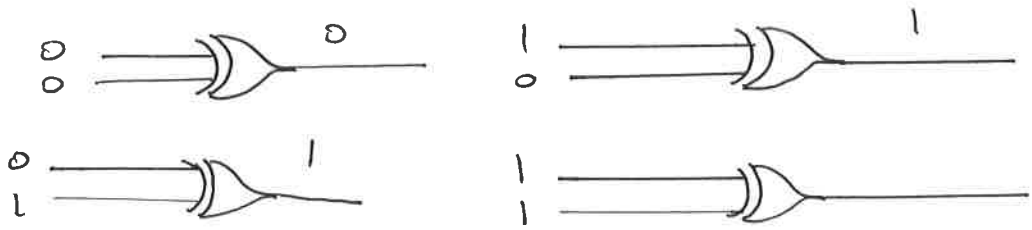
For example if we compare A and B

(I/P No.) A	B	z_1 (A>B)	z_2 (A<B)	z_3 (A=B)
0	0	0	0	1
0	1	0	1	0
1	0	1	0	0
1	1	0	0	1

From truth table

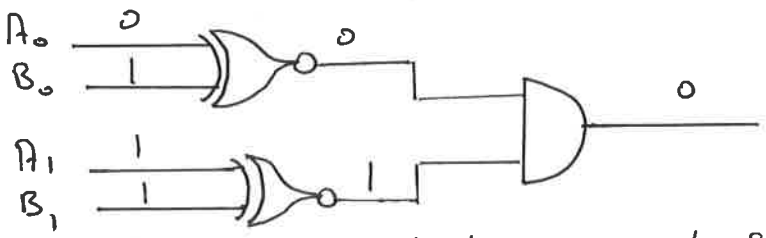
$$z_1 = A\bar{B}$$
$$z_2 = \bar{A}B$$
$$z_3 = \bar{A}\bar{B} + AB = A \odot B$$

The main Gate which is used to build the comparator is (EX-OR) which is:-

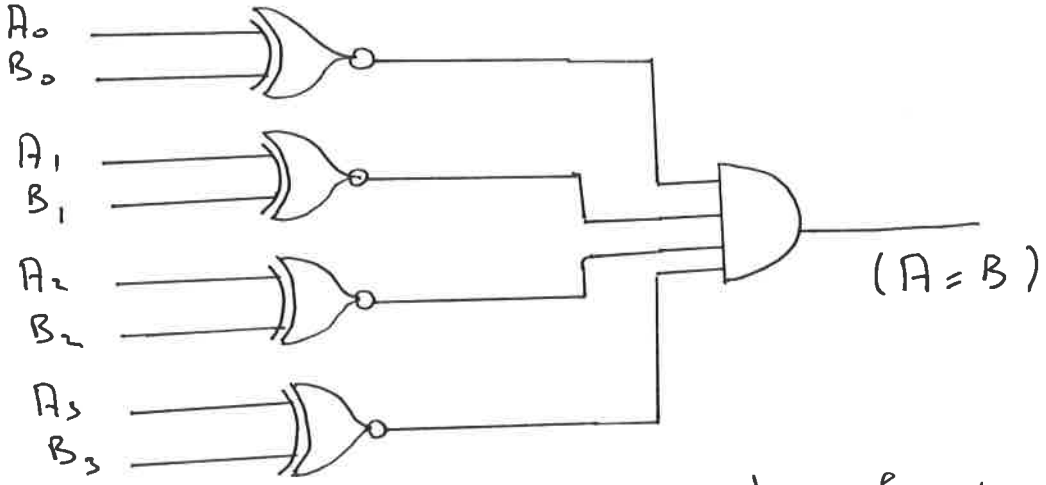


when we have numbers has two bits (MSB , LSB).

MSB LSB
A = A_1 A_0
MSB LSB
B = B_1 B_0



If the numbers have Four bits, which we need four (Ex-OR).



The (7485) Ic is a comparator for two numbers, have four bits.